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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/085,799	02/26/2002	Gregory C. Parrish	42P13912	8022

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EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	5

DATE MAILED: 06/28/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 10/085,799	Applicant(s) PARRISH, GREGORY C.	
	Examiner James C Kerveros	Art Unit 2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☒ Claim(s) *10,11 and 14-20* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *28 May 2002* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the present U.S. Application filed February 26. Claims 1-20 are now pending and are hereby presented for examination

Drawings

2. The drawings are objected to because of shaded areas and non- legible handwritten characters, in FIGS 1-3.

Corrected drawing sheets are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

3. The abstract of the disclosure is objected to because the abstract does not adequately describe the claimed invention. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details. Correction is required. See MPEP § 608.01(b).

Claim Objections

4. Claims 10, 11 and 14-20 are objected to because of the following informalities:

Claim 10, on line 1, the term "decompressed" should be changed to "compressed" because of antecedent basis with the term "compress at least one of the plurality of outputs" recited in claim 9. Appropriate correction is required.

Claims 11 and 15, a period should be added at the end of claim.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Shiraishi (US 6556037).

Regarding independent Claims 1, 9 and 15, Shiraishi discloses a method and a system for testing a unit (Device Under Test, DUT, LSI 300) comprising:

Receiving a compressed test vector (step S303) by the unit (DUT, LSI 300) from the tester (350), which loads the compressed test pattern for the test controller (330) from the EWS (step S302), as shown in FIG. 6 and FIG. 7 block diagram and flowchart for testing of a semiconductor integrated circuit.

Decompressing a compressed test vector, using test controller (330) which decompresses the compressed test pattern in the scan test format received from the tester 350 via the virtual (SI pin P310) by the pattern decompressing unit 332 and generates an input pattern for the input pin to the core logic 310 in the LSI 300 (step S304).

Generating a compressed test vector output from the unit (LSI 300) DUT, using compressing unit 333 (step S308) for further compressing the output pattern and also using the test controller 330 to output the encoded compressed output pattern to the tester 350 via the virtual SO pin P320, (step S309).

Regarding Claims 2 and 4, Shiraishi discloses compressing an output by the unit using compressing unit 333 (step S308) and forwarding the compressed output to a test platform (tester 350) via the virtual SO pin P320, (step S309), wherein bypassing the compression if the output does not efficiently compress, including the (step S308) of using the test controller 330 to reconstruct the output pattern by discarding unnecessary

data, which encodes the reconstructed output pattern into an output pattern in the scan test format.

Regarding Claims 5, 11 and 19, Shiraishi discloses functional test pattern for testing the function of the unit (Device Under Test, DUT, LSI 300).

Regarding Claims 6 and 16, Shiraishi discloses receiving the compressed test vector (step S303) by the unit (DUT, LSI 300) from the tester (350), including the step of loading the compressed test vector via a single pin virtual (SI pin P310), FIG. 6.

Regarding Claims 7,12 and 18, Shiraishi discloses unit (DUT, LSI 300), which is an integrated device.

Regarding Claims 8, 13 and 14, Shiraishi discloses a test platform, comprising workstation (EWS) coupled to automatic test equipment (tester 350).

Regarding Claim 10, Shiraishi discloses analysis logic (tester 350) for receiving the compressed output via virtual scan-out (SO) pin P320.

Regarding Claim 20, Shiraishi discloses pattern-compressing unit 333 (step S308), which compress the output from the core logic 310 via BSR 320.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraishi (US 6556037).

Regarding Claim 3, bypassing the decompression if the test vector does not efficiently compress. However, Shiraishi discloses the method step of discarding unnecessary data in the output patterns obtained via the BSR 320, thereby encoding the input test pattern into a test pattern in the scan test format and, after that, the test pattern is compressed. It would have been obvious to a person having ordinary skill in the art at the time the invention was made to bypass the decompression by discarding unnecessary data in the output patterns obtained via the BSR 320, as taught by Shiraishi, as to efficiently decompress all the valid test vectors of the input test pattern to the DUT.

8. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over Shiraishi (US 6556037) in view of Applicant's own admitted prior art.

Regarding Claim 17, Shiraishi does not disclose a delta method decompression protocol supported by the decompression logic. However, Applicant's own admitted prior art states that the decompression logic decompresses all the test vectors utilizing a well-known decompression method known as "delta method". It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a well-known decompression method known as "delta method", as taught by

Applicant's own admitted prior art, in the Shiraishi's decompressing unit 332, as to efficiently decompress all the valid test vectors of the input test pattern to the DUT.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Rajski et al. (US 6684358) discloses the claimed limitations (FIG. 2) including compressed test patterns (32) being provided by the tester 21 to the input channels of the decompressor / PRPG 36, which decompresses the compressed pattern into a decompressed pattern of bits, then applied to the scan chains 26 in the CUT 24 and then the test response to that pattern is captured in the scan chains and passed to the MISR 42, where it is compressed compacted as part of a signature.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James C Kerveros whose telephone number is (703) 305-1081. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status

information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

By: _____

U.S. PATENT OFFICE
Examiner's Fax: (703) 746-4461
Email: james.kerveros@uspto.gov

Date: 23 June 2004
Office Action: Non-Final Rejection

James C Kerveros
Examiner
Art Unit 2133

Guy J. Lamarre
for
Albert DeCady
Primary Examiner